Abstract of the Invention

A COMPUTER SYSTEM WITH DEBUG FACILITY

A computer system with enhanced integrated debug facilities is described. According to one aspect, step-by-step execution of an instruction sequence is implemented where each instruction is guarded. If, after guard resolution, the instruction is committed, a divert routine is executed. If the instruction is not committed, the next instruction in the sequence is executed.

According to another aspect, a stall state can be set at the decode unit either by reading stall attributes associated with debug instructions, or responsive to a stall command from an on-chip emulation unit.